**In the Specification:**

At page 7, lines 19 – 32 and page 8, lines 1 - 17, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

In a still further embodiment of the present invention, the second timer is a second binary counter and has M+1 bits, where M is less than or equal to N, to produce a second time interval having a duration less than or equal to the first time interval. For example, to sample events within a 1 microsecond window within each 1 millisecond time range using a 1 GHz clock rate, a 20 bit (plus 1 overflow bit) first timer count register provides a 1 millisecond first time interval, a 10 bit (plus 1 overflow bit) second timer count register provides a 1 microsecond second time interval (timing window within each 1 millisecond first time interval). A pseudo-random number generator having a 5 bit counter is used to populate a 20 bit latch register. In another example embodiment, the first timer is adapted to time a series of periodic first time intervals, for example, by resetting and/or restarting the first timer after each first time interval times out. The delay timer is adapted to determine a new delay time for each first time interval, for example, by forming a new N bit pseudo-random number prior to each first time interval. The new delay time is not prohibited from being the same as the previous delay time. In a further example embodiment, a counting circuit is coupled to the output terminal of the coincidence circuit. The counting circuit includes the counting circuits described in ~~the co-pending application entitled,~~ "Analog Method and Circuit for Monitoring Digital Events Performance," by Joseph Weiyeh Ku, ~~docket number 10013825-1 (attorney docket number HPCO.076PA).~~ U.S. Patent Number 6,600,328 B2, July 29, 2003. In a further example embodiment, the counting circuit is reset responsive to a reset signal derived from a first timer value. For example, the reset signal is derived from the first timer's most significant bit in one embodiment, and derived from a first timer overflow bit in another embodiment. In a still further example embodiment, the reset signal derived from first timer is supervised by external logic (not shown) blocking reset at the end of one or more base time intervals and allowing the counting circuit to accumulate a count over a plurality of sampling window intervals. For example, in the case of a "low event count," where an accumulated count does not exceed some minimum threshold, the counting circuit is not reset at the end of the base time interval. In an alternative example embodiment of the present invention, a counting circuit reset signal is derived from external logic (not shown) and not derived from the first timer at all enabling count accumulation over a plurality of sampling window

intervals. In another alternative embodiment, the reset signal is associated with the end of the sampling window interval.

At page 13, lines 13 – 19, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

In one example embodiment, coincidence circuit 250 is an AND gate. Coincidence circuit 250 has an output terminal 258 coupled to a counting circuit 360. In one example embodiment, counting circuit 360 is a digital counter, such as a binary count register. In another example embodiment, counting circuit 360 is an analog circuit as described in ~~the co-pending application entitled,~~ "Analog Method and Circuit for Monitoring Digital Events Performance," by Joseph Weiyeh Ku, ~~docket number 10013825-1 (attorney docket number HPCO.076PA).~~ U.S. Patent Number 6,600,328 B2, July 29, 2003.